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DAVID H HITT
HITT CHWANG & GAINES
225 UNIVERSITY PLAZA
275 WEST CAMPBELL ROAD
RICHARDSON, TX 75080

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DONAGHUE, LARRY D	
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BEFORE THE BOARD OF PATENT APPEALS

AND INTERFERENCES

Paper No. 10

Application Number: 09/213,970

Filing Date: 12/17/1998

Appellant(s): Diepstraten et al.

David H. Hitt

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 11/18/02.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

5,528,513	VAITZBLIT et al.	06-1996
6,009,454	DUMMERMUTH	12-1999
6,085,218	CARMON	7-2000
5,239,652	SEIBERT et al.	8-1993
5,713,038	MOTOMURA	1-1998

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4, 5, 7, 8, 11, 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vaitzblit et al. (5,528,513) in view Dummermuth et al. (6,009,454) .

Vaitzblit et al. taught the invention (1, 5) substantially as claimed including a foreground controller (figure 1, 158) for activating the task according to priority (see abstract) and in response to events (see abstract, particularly lines 8-9, invoked by timer interrupt for each task is an event), and a background controller operating in a cyclical manner (col. 5, lines 15-17 and Figure 1, 100).

Dummermuth et al. taught a controller for cyclicly activates context according to the number on instruction executed (col. 7, lines 23-35; col. 3, lines 19-25) and a counter that counts the number of executed with respect to a given task (col. 7, lines 23-34 and col. 3, lines 40-45).

As to claim 4, Dummermuth et al. taught vectoring to a selectable memory location (col. 8, lines 34-38).

As to claim 7, Dummermuth et al. taught that the application task contained the information as to how many instruction to execute (col. 8, lines 4-14, and 44-49) and the suggest to implement in hardware (col. 7, lines 23-34).

Dummermuth et al. did not expressly discloses the application of the task control system to background task. It would have been obvious to one of ordinary skill in the art to apply the teaching of Dummermuth et al. to background task, to gain the benefit of precise allocation of processor resources according to how many of instructions are to be executed in each task as opposed to how much time.

Claims 8, 11 and 14 fail to teach or define above or beyond claims 1, 4, and 7 and are rejected for the reasons set forth above.

2. Claims 2, 6 , 9 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vaitzblit et al. (5,528,513) and Dummermuth et al. (6,009,454) as applied to claims 1 and 8 above, and further in view of Carmon (6,085,218).

Vaitzblit et al. and Dummermuth et al. did not expressly disclose the use of a register on a processor or the decrementing the register to determine the task switch. It would have been obvious to one of ordinary skill in the data processing art to combine these references in view of the express suggestion of Dummermuth et al. to use specialized hardware to perform the operation.

As to claims 6 and 13, Carmon taught the use of the register (col. 3, lines 14-20, figure 1).

As to claims 2 and 9, Carmon taught decrementing the register (col. 3, lines 14-20, figure 1).

3. Claims 3 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vaitzblit et al. (5,528,513) and Dummermuth et al. (6,009,454) as applied to claims 1 and 8 above, and further in view of Seibert et al. (5,239,652).

Dummermuth et al. failed to disclose placing the processor in an idle state. Seibert et al. taught place a processor in idle state in response to inactivity. It would have been obvious to combine the teachings to allow for the reduction of power consumption.

4. Claims 15, 18, 19 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vaitzblit et al. (5,528,513) and Dummermuth et al. (6,009,454) as applied to claims 1, 4, 7, 8, 11 and 14 above, and further in view of Motomura (5,713,038).

Dummermuth et al. taught the invention substantially as claimed including a controller for cyclicly activates context according to the number on instruction executed (col. 7, lines 23-35; col. 3,

lines 19-25) and a counter that counts the number of executed with respect to a given task (col. 7, lines 23-34 and col. 3, lines 40-45).

Vaitzblit et al. and Dummermuth et al. did not teach a plurality of register sets and the interconnection of the plurality of register sets with the execution core. Motomura taught the use of a plurality of register sets and the interconnection of the plurality of register sets with the execution core. It would have been obvious to one of ordinary skill in the data processing art to modify the teaching of Dummermuth et al. with that of Motomura to realize high speed and more flexible context switching, in an conventional processor.

As to claim 18, Dummermuth et al. taught vectoring to a selectable memory location (col. 8, lines 34-38).

As to claim 21, Dummermuth et al. taught that the application task contained the information as to how many instruction to execute (col. 8, lines 4-14, and 44-49) and the suggest to implement in hardware (col. 7, lines 23-34).

As to claim 22, It would have obvious to one of ordinary skill in the data processing art to included the teaching of Dummermuth et al. and Motomura, to gain the benefit of precise allocation of processor resources according to how many of instructions are to be executed in each task as opposed to how much time and to realize high speed and more flexible context switching, in an general-purpose computer.

5. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vaitzblit et al. (5,528,513) , Dummermuth et al. (6,009,454) and Motomura (5,713,038) as applied to claim 15 above, and further in view of Seibert et al. (5,239,652).

The combined teachings failed to disclose placing the processor in an idle state. Seibert et al. taught place a processor in idle state in response to inactivity. It would have been obvious to combine the teachings to allow for the reduction of power consumption.

6. Claims 16 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vaitzblit et al. , Dummermuth et al. (6,009,454) and Motomura (5,713,038) as applied to claim 15 above, and further in view of Carmon (6,085,218).

Vaitzblit et al. , Dummermuth et al. and Motomura did not expressly disclose the use of a register on a processor or the decrementing the register to determine the task switch. It would have been obvious to one of ordinary skill in the data processing art to combine these references in view of the express suggestion of Dummermuth et al. to use specialized hardware to perform the operation.

As to claim 16, Carmon taught the use of the register (col. 3, lines 14-20, figure 1).

As to claim 20, Carmon taught decrementing the register (col. 3, lines 14-20, figure 1).

(11) Response to Argument

A. The Examiner rejected Claims 1, 4, 7, 8, 11 and 14 under 35 U.S.C. §103(a) as being unpatentable over Vaitzblit in view of Dummermuth. The Examiner asserts that Vaitzblit teaches the invention substantially as claimed including a background controller operating in a cyclical manner. The Appellants respectfully disagree.

B. In Vaitzblit, there maybe many general-purpose class tasks in a server 20, all of which need to make progress in order for the server 20 to function. The general-purpose tasks, therefore, are granted a minimum CPU processing quantum to ensure that general-purpose tasks can always make progress.

(Column 3, lines 33-43). The general-purpose tasks that are ready for execution are placed on a general-purpose ready queue 108, which is served in a round-robin fashion. If the general-purpose ready queue 108 is not empty, the scheduler 53 starts a general-purpose quantum timer, and activates the first task from the general-purpose ready queue 108. (Column 5, lines 1522).

C. The first task in the general-purpose ready queue runs until it blocks or the quantum timer expires. If the task blocks, its context is saved on a wait queue and the first task from the general purpose ready queue is restored for execution. If the quantum timer expires, the scheduler 53 saves the context of the currently running task at the end of the GP ready queue and switches to a new round of servicing the real-time tasks. The execution of the general-purpose tasks may be preempted one or more times by the isochronous tasks. After each preemption, the execution of the general-purpose class continues until the total time spent in processing general-purpose tasks reaches the guaranteed quantum. (Column 5, lines 22-32).

D. The scheduler, however, does not cyclicly activate a context corresponding to another background task when the number of executed instructions of a given background task equals a dynamically-programmable time slice value. (Claims 1 and 8). Instead, the scheduler processes another general-purpose task after processing of a first general-purpose task is complete and the quantum timer has not expired. Additionally, the scheduler will switch from processing a general purpose task to processing an isochronous task when preempted. Finally, the scheduler will switch to processing a real-time task when the quantum timer expires. Vaitzblit, therefore, teaches switching between general-purpose tasks when processing of the first task is complete (block) and the quantum timer has not expired. Vaitzblit does not teach or suggest, however, cyclicly activating a context corresponding to another background task when

the number of instructions executed with respect to a given background task equals a dynamically-programmable time slice value as recited in independent Claims 1 and 8.

In response to paragraphs A-D: Appellant can not show non-obviousness by attacking the references individually where, as here the rejection(s) are based on a combination of references. See: In re Keller, 208 USPQ 871 (CCPA)1981. Further the requirements of 35 U.S.C. 103(a), nor has court precedent established that for the rejection to be proper that the teachings of the reference be limited only to claimed subject matter of the application to which it is applied as prior art. Appellant has addressed various passages in Vaitzblit reference that go beyond the scope of the claimed subject matter of the instant application, this does not invalidate the rejection.

The Examiner also asserts that Dummermuth teaches a controller that cyclicly activates context according to a number of instruction executed and a counter that counts the number of executed instructions with respect to a given task. (Examiner's Action mailed on June 18, 2002, page 2). Dummermuth, however, does not teach a context controller that cyclicly activates a context corresponding to a background task when the number of instructions executed with respect to another background task equals a dynamically-programmable time slice value. (Claims 1 and 8).

In response: Note that Appellant has defined in the instant application dynamically programmable to mean " being programmable subsequent to system initialization" ; page 19, lines 12-13. Therefore as counters are programmed by writing a value into the count register, to meet the requirements of the claim limitation, the value of the counter would merely have a new value written into the count register during the operation of the system. In essence the Appellant is

alleging that his patentable subject matter is sharing a piece of hardware, the underlying principle of multi-tasking, having multiple task or processes appear to be running simultaneously on the same hardware. Again, Appellant can not show non-obviousness by attacking the references individually where, as here the rejection(s) are based on a combination of references. See: In re Keller, 208 USPQ 871 (CCPA)1981.

Dummermuth discloses a multi-tasking operating system for real-time control of industrial processes. (Abstract). Multi-tasking is provided by recognizing that both ladder-type and state-type programs can be considered as simply a collection of individual instructions linked together by an implicit pointer list. At the conclusion of any instructions, a pointer may be developed to a single next instruction. (Column 2, lines 48-53). The operating system "switches between tasks after a predetermined number of instructions by making the execution of each instruction explicit." (Column 7, lines 23-26). This differs from the present invention where a slice value is dynamically programmable instead of predetermined.

In response: Again note that Appellant has defined in the instant application dynamically programmable to mean " being programmable subsequent to system initialization" ; page 19, lines 12-13. Therefore as counter are programmed by writing a value into the count register, to meet the requirements of the claim limitation, the value of the counter would merely have a new value written into the count register during the operation of the system. In essence the Appellant is alleging that his patentable subject matter is sharing a piece of hardware, the underlying principle of multi-tasking, having multiple tasks or processes appear to be running simultaneously on the same hardware. Further, Appellant can not show non-obviousness by attacking the references individually where, as here the rejection(s) are based on a combination of references. See: In re Keller, 208 USPQ

871 (CCPA)1981. The appellant is reminded that the courts have held, not only the specific teachings of a reference but also reasonable inferences which an artisan would have logically drawn therefrom may be properly evaluated in formulating a rejection. *In re Preda*, 401 F.2d 825, 159 USPQ 342 (CCPA 1968) and *In re Sherpard*, 319 F.2d 194, 138 USPQ 148 (CCPA 1963).

Dummermuth taught that the process could be done through specialized hardware (col. 7, lines 25-28).

Although this ***tracking of the number of executed instructions could be done through specialized hardware*** *that reads the instruction counter of the processor of the processor module 30...*

Dummermuth suggest the use of a counter (col. 3, lines 40-45).

Most processing hardware does not provide an internal count of the number of instructions that it has executed that may be used to trigger a task switching operation.

Therefore the Dummermuth suggest as an alternative embodiment the use of the counter, which one of ordinary skill in the art, would be aware would be written to change the value for each task. Further appellant appears to be arguing that proggrammable hardware is a novel feature in the data processing art.

Since neither Vaitzblit nor Dummermuth teach or suggest cyclicly activating a context corresponding to another background task when the number of instructions executed with respect to a given background task equals a dynamically-programmable time slice value as recited in independent Claims 1 and 8, the Examiner cannot establish a *prima facie* case of obviousness of Claims 1 and 8 and Claims dependent thereon. Accordingly, the Appellants

respectfully traverse the Examiner's rejection of Claims 1, 4, 5, 7, 8, 11, 12 and 14 under 35 U.S.C. § 103(a) and request a reversal of the Examiner's rejection with respect to these claims.

In response: This is a mere allegation of patentable, without addressing the technical merits of the rejection.

Furthermore, the combination of Vaitzblit and Dummermuth is improper. As the board understands, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is a teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. In *re Fine, .5 U.S.P.Q. 2d 1596 (1998).* The motivation to combine references may ". . . come from the nature of a problem to be solved, leading inventors to look for references relating to possible solutions to that problem." *Pro-Mold and Tool Company v. Great Lakes Plastics Inc.* 37 U.S.P.Q.2d 1626 (1996). However, hindsight is never appropriate motivation for combining references. To this end, relying upon hindsight knowledge of the Appellant's disclosure when the prior art does not teach nor suggest such knowledge, results in the use of the invention as a template for its own reconstruction. This is inappropriate in the determination of patentability. *Sensonics Inc. v. Garlock, Inc.* 220 U.S.P.Q. 303 (1983).

In Response: Dummermuth expressly taught replacing how much time each task is allocated, with how many instructions are to be executed in each task (col. 3, lines 19-25).

It is thus one object of the invention to provide a multi-tasking system suitable for industrial control in that ***it permits the precise allocation of processor resources according to how many instructions are to be executed in each task as opposed to how much time each task is allotted****. The task programs may be ladder-type programs or state-type programs.*

One skilled in the art would not be motivated to combine Vaitzblit with Dummermuth to arrive at the claimed invention because Vaitzblit is directed to a scheduler for a continuous media file server and Dummermuth is directed to a multi-tasking operating system for real-time control of industrial processes. More specifically, Vaitzblit is directed to solving the problem of scheduling multiple classes of tasks with diverse performance requirements for use in continuous media applications and Dummermuth is directed to solving the multi-tasking of special purpose computers uniquely suited for the industrial controller environment.

In response: It should be noted that Appellant is differentiating the reference by intended use. The fact of the matter is that both references are directed to multi-tasking scheduling systems. Further Dummermuth expressly provides motivation for the combination (col.3, lines 19-25). Appellant has mischaracterized the relevance of

the Dummermuth reference, all scheduler control something beyond themselves. Appellant allegations would lead to the conclusion the only applicable art would be references that control the same operation; appellant has failed to claim any operation. Further, the scheduling computer is a general purpose computer as expressly taught by Dummermuth (col. 5, lines 1-4).

The Examiner rejected Claims 2, 6, 9 and 13 under 35 U.S.C. § 103(a) as being unpatentable over Vaitzblit and Dummermuth in view of Carmon. Neither Vaitzblit nor Dummermuth, however, individually or in combination, teach or suggest each and every element of independent Claims 1 and 8. Furthermore, Carmon does not cure the deficiencies of Vaitzblit and Dummermuth. Instead, Carmon is directed to monitoring a multi-task system by detecting overrun of any task beyond a declared maximum processor cycle limit for the task. (Abstract). Since the Examiner did not establish a *prima facie* case of obviousness of independent Claims 1 and 8, and Carmon does not cure the deficiencies of Vaitzblit and Dummermuth, then the Examiner cannot establish a case of obviousness of dependent Claims 2, 6, 9 and 13. Accordingly, the Applicants respectfully traverse the Examiner's rejection of Claims 2, 6, 9 and 13 under 35 U.S.C. §103(a) and request a reversal of the Examiner's rejection with respect to these claims.

In response: This is a mere allegation of patentable, without addressing the technical merits of the rejection.

The Examiner rejected Claims 3 and 10 under 35 U.S.C. § 103(a) as being unpatentable over Vaitzblit and Dummermuth in view of Seibert. Neither Vaitzblit nor Dummermuth, however, individually or in combination, teach or suggest each and every element of independent Claims 1 and 8. Furthermore, Seibert does not cure the deficiencies of Vaitzblit and Dummermuth. Instead, Seibert is directed to reducing the power consumption of a computer by determining when the central processing unit is not actively processing and generating a power-off signal to a control logic circuit. (Abstract). Since the Examiner did not establish a prima facie case of obviousness of independent Claims 1 and 8, and Seibert does not cure the deficiencies of Vaitzblit and Dummermuth, then the Examiner cannot establish a case of obviousness of dependent Claims 3 and 10. Accordingly, the Applicants respectfully traverse the Examiner's rejection of Claims 3 and 10 under 35 U.S.C. §103(a) and request a reversal of the Examiner's rejection with respect to these claims.

In response: This is a mere allegation of patentable, without addressing the technical merits of the rejection.

The Examiner rejected Claims 15, 18, 19 and 21-22 under 35 U.S.C. §103(a) as being unpatentable over Vaitzblit and Dummermuth in further view of Motomura. As discussed above with respect to independent Claims 1 and 8, Vaitzblit and Dummermuth do

not teach or suggest switching between background tasks using a dynamically-programmable time slice value as claimed in independent Claim 15. Furthermore, Motomura does not cure the deficiencies of Vaitzblit and Dummermuth. Instead, Motomura is directed to a microprocessor that has a register file which allows a higher speed, more flexible, context switching as compared to conventional microprocessors. (Column 3, lines 15-17). Since Vaitzblit and Dummermuth do not teach each and every element of independent Claim 15 and Motomura does not cure its deficiencies, then the Examiner can not establish a prima facie case of obviousness of independent Claim 15 and Claims dependent thereon. Accordingly, the Applicants respectfully traverse the Examiner's rejection of Claims 15, 18, 19 and 21-22 under 35 U.S.C. §103(a) and request a reversal of the Examiner's rejection with respect to these claims. Furthermore, a person having ordinary skill in the art could not have arrived at the processor claimed in Claim 15 by combining the teachings of Vaitzblit, Dummermuth and Motomura since neither Vaitzblit, Dummermuth or Motomura teach or suggest switching between tasks using a dynamically programmable time slice value.

In response: This is a mere allegation of patentable, without addressing the technical merits of the rejection.

The Examiner rejected Claim 17 under 35 U.S.C. §103(a) as being unpatentable over Vaitzblit, Dummermuth and Motomura and further in view of Seibert. As stated above, Vaitzblit and Dummermuth do not teach or suggest each and every element of independent

Claim 15. Furthermore, neither Motomura or Seibert cure the deficiencies of Vaitzblit and Dummermuth. No combination, therefore, of Motomura, Seibert, Vaitzblit, or Dummermuth teaches or suggests each and every element of Claim 17. The Examiner, nevertheless, cannot establish a prima facie case of obviousness with respect to Claim 17 which includes each element of independent Claim 15. Accordingly, the Applicants respectfully traverse the Examiner's rejection of Claim 17 under 35 U.S.C. § 103(a) and request a reversal of the Examiner's rejection with respect to these claims.

In response: This is a mere allegation of patentable, without addressing the technical merits of the rejection.

The Examiner rejected Claims 16 and 20 under 35 U.S.C. § 103(a) as being unpatentable over Vaitzblit, Dummermuth and Motomura and in further view of Can-non. Neither Vaitzblit nor Dummermuth teach or suggest each and every element of independent Claim 15. Furthermore, neither Motomura or Cannon cure the deficiencies of Vaitzblit and Dummermuth. No combination, therefore, of Motomura, Vaitzblit, Cannon or Dummermuth teaches or suggests each and every element of Claims 16 and 20. The Examiner, nevertheless, cannot establish a prima facie case of obviousness with respect to Claims 16 and 20. Accordingly, the Applicants respectfully traverse the Examiner's rejection of Claims 16 and 20 under 35 U.S.C. § 103(a) and request a reversal of the Examiner's rejection with respect to these claims.

In response: This is a mere allegation of patentable, without addressing the technical merits of the rejection.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

LARRY D. DONAGHUE
PRIMARY EXAMINER

Larry Donaghue

December 6, 2001

Conferee
Patrice Winder
Patrice Winder